LCD Display Driver Chip CH463

Datasheet

Version: V1.0

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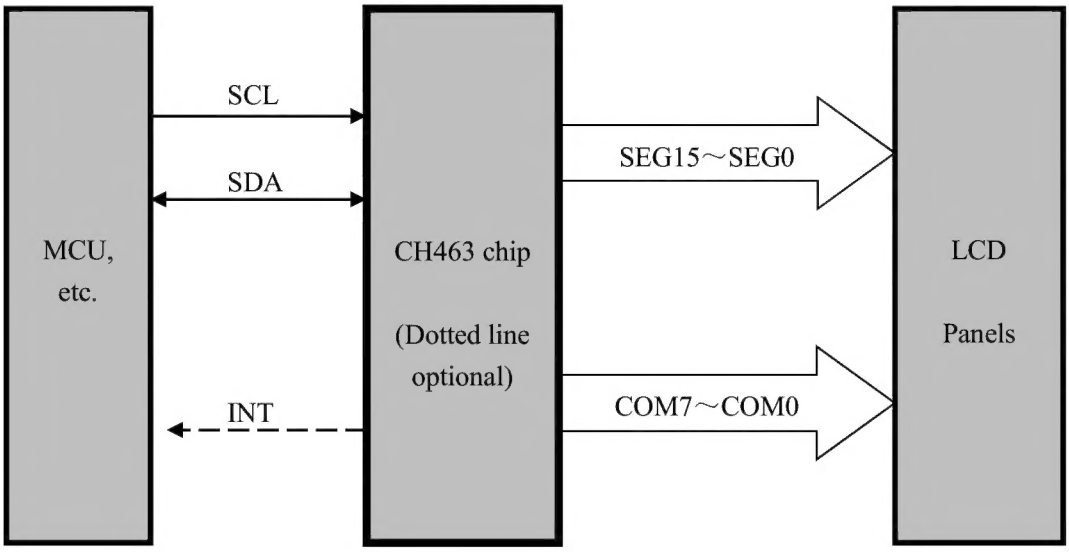
1. Overview

CH463 is a display driver chip of LCD. CH463 has a built-in clock oscillator circuit and supports LCD panels of 128 points (16×8), 48 points (12×4), etc., and also allows keyboard scanning of 35 keys (based on a 7×5 matrix); CH463 exchanges data with microcontrollers, etc., through a 2-wire serial interface.



2. Features

2.1 Display Driver

- Support LCD panels up to 16×8, 16 SEGs, and 8 COMs.
- Support LCD specifications such as 1/4 duty, 1/3 bias or 1/8 duty, 1/4 bias.
- Support frame rate adjustment.
- Built-in bias circuit and external VLCD pin for LCD working voltage adjustment.
- Provide 64 levels of PWM for LCD backlight adjustment.

2.2 Keyboard Control

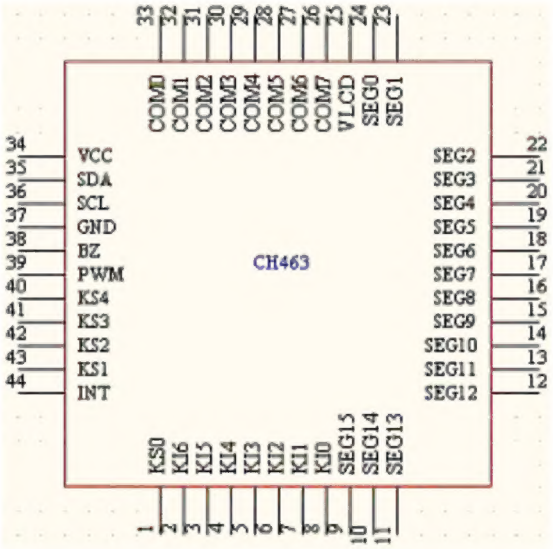
- Built-in 35-key keyboard controller, based on 7×5 matrix keyboard scanning.
- Built-in pull-up resistor for key status input, built-in de-jitter circuit.
- Keyboard interrupt output, active low.
- Support key combination.

2.3 Other Miscellaneous

- Provide GPIO universal input and output expansion pins (pins not used for keyboard scan matrices).
- 2-wire serial interface, compatible with I2C bus, saving pins.
- Provide buzzer driver output, 2 frequencies are optional.

- Built-in clock oscillation circuit, no need to provide external clock or external oscillation components, more anti-interference.
- Provide LQFP44 no-lead package, compatible with RoHS.

3. Package



Package form	Body size		Pin pitch		Package description	Order model
LQFP44	10*10mm		0.8mm	31.5mil	Low Profile Quad Flat Pack	CH463Q

4. Pins

Pin No.	Pin name	Pin type	Pin description
34	VCC	Power	Working power supply input
37	GND	Power	Common ground
25	VLCD	Power	LCD power supply input
9~24	SEG15~SEG0	Output	LCD SEG driver port
26~33	COM7~COM0	Output	LCD COM driver port
40~43,1	KS4~KS0	Keyboard output	Keyboard scan output port, GPIO pin,
2~8	KI6~KI0	Keyboard input	Keyboard scan input port, GPIO pin, built-in pull-up resistor
35	SDA	Open-drain output and input	Data input and output of 2-wire serial interface, built-in pull-up resistor
36	SCL	Input	Data clock of 2-wire serial interface, built-in pull-up resistor
44	INT	Open-drain output	Keyboard interrupt output, active at low level, built-in pull-up resistor
38	BZ	Output	Buzzer drive output
39	PWM	Output	PWM output, which can be used for LCD backlight drive

5. Register Space

For the data in this manual, the data ending in B is a binary number, and that ending in H is a hexadecimal number, otherwise it is a decimal number, and the bit marked with x indicates that the bit can be any value.

Description: Reserved bits are ignored when reading and 0 is written when writing.

Address	Read/write (R/W)	Register description
00H~0FH	R/W	Display memory for LCD, see section 6.1 for correspondence
40H	R/W	Reset register, Bit0 indicates reset, write 1 performs reset operation, reset completes automatic zeroing, other bits remain undefined
41H	R/W	Function setting register: Bit0: 1, LCD display enable; 0, disable Bit1: 1, keyboard scan enable; 0, disable Bit2: 1, PWM output enable; 0, disable Bit3: 1, BZ output enable; 0, disable Other bits remain undefined
42H	R/W	LCD frame frequency adjustment register: LCD frame frequency =Fosc/2/2/ (the value of adjustment register +1)/duty/(1 or 2), A-type divided by 2, B-type divided by 1
43H	R/W	Keyboard scan frequency adjustment register (only 0 to 15 are active): Scanning frequency =Fosc/2/2/ (the value of adjustment register +1)/8/5,
44H	R/W	LCD configuration register, see section 6.1
45H	R/W	PWM configuration register, see section 6.3
46H	R/W	BZ configuration register, see section 6.3
47H	R	Interrupt state register, Bit0 is 1 indicates a change in keys Automatic clear after reading key value, and other bits remain undefined
48H	R/W	GPIO enable of KI: 1, enable GPIO; 0, disable GPIO, see Section 6.3
49H	R/W	GPIO enable of KS: 1, enable GPIO; 0, disable GPIO, see Section 6.3
4AH	R/W	GPIO output enable of KI, see Section 6.3
4BH	R/W	GPIO output enable of KS, see Section 6.3
4CH	R/W	GPIO pull-up enable of KI, see Section 6.3
4DH	R/W	GPIO pull-up enable of KS, see Section 6.3
4EH	R/W	Output register and input state register of KI: It is the output state when GPIO is enabled by KI during writing Current state of KI pins during reading See Section 6.3
4FH	R/W	Output register and input state register of KS, PWM and BZ: It is the output state when GPIO is enabled by KS and (PWM, BZ) during writing, Current state of KS and (PWM, BZ) pins during reading,

		See Section 6.3
50H~52H	R	Key value register: 00H: Indicate key release, 01H: Indicate key error, For detailed key values, see Section 6.2.

6. Function Description

6.1 LCD Display Driver

CH463 has built-in 16 × 8-bit data storage, and the address is from 00H to 16-byte units of 0FH, corresponding to the LCD points connected to SEG and COM pins, respectively. The corresponding relationship is as follows:

Addressing	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
SEG0(00H)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEG1(01H)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEG2(02H)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEG3(03H)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEG4(04H)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEG5(05H)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEG6(06H)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEG7(07H)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEG8(08H)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEG9(09H)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEG10(0AH)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEG11(0BH)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEG12(0CH)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEG13(0DH)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEG14(0EH)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEG15(0FH)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

The Bit0 of address 41H is the LCD driver enable bit. The position 1 enables LCD display and closes when it is set to 0.

Address 42H is the LCD frame frequency adjustment register, LCD frame frequency = Fosc/2/2/ (the value of the adjustment register + 1) / duty/ (1 or 2), A-type divided by 2 and B-type divided by 1.

Address 44H is the LCD configuration register, where Bit3 and Bit7 are reserved values, and Bit6 is the type of output waveform: 0 is A-type, 1 is B-type. The detailed configuration is shown in the following table:

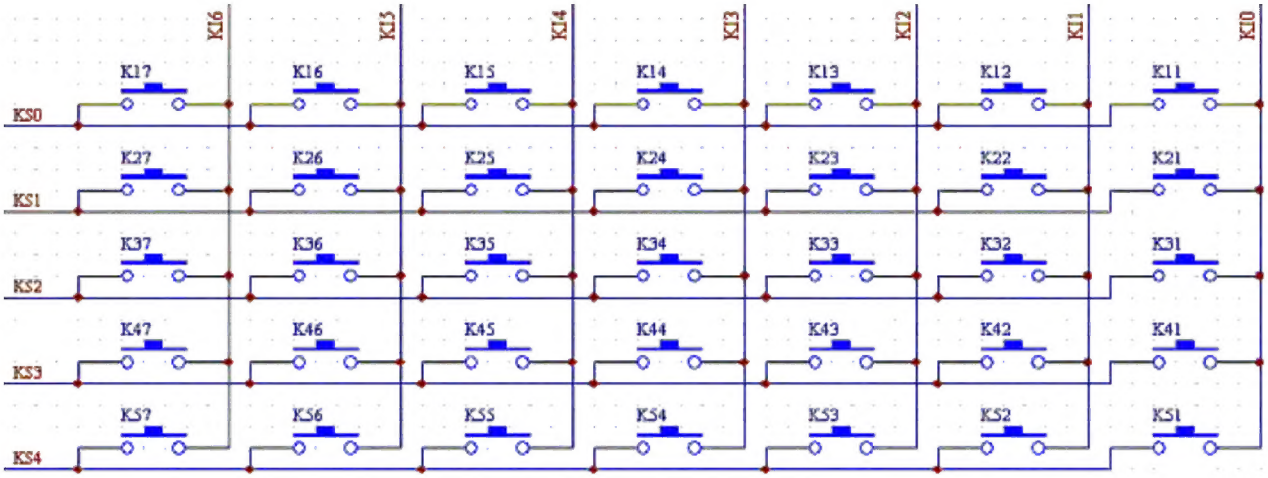
Bit2	Bit1	Bit0	Duty
0	0	0	1/1 Duty
0	0	1	1/2 Duty
0	1	0	1/3 Duty
0	1	1	1/4 Duty
1	0	0	1/5 Duty
1	0	1	1/6 Duty
1	1	0	1/7 Duty

1	1	1	1/8 Duty

Bit5	Bit4	Bias
0	0	1/4 bias
0	1	Reserved, undefined
1	0	1/2 bias
1	1	1/3 bias

6.2 Keyboard Scanning

The scan matrix of CH463 is 7 × 5, as shown in the following figure:



The Bit1 of address 41H is the keyboard scanning enable bit, which enables keyboard scanning at 1 and turns off at 0.

Address 43H is the keyboard scan frequency adjustment register (valid only from 0 to 15), scan frequency = Fosc/2/2/ (value of the adjustment register + 1)/8/5.

During the scanning process, if a key on the keyboard changes (press or release), the Bit0 at address 47H will be set to 1, and the INT pin will output a low level, and when the user reads the key value, the Bit0 at address 47H will automatically zero, and the INT pin will output a high level. Support any two-key combination and 3-key combination without keystroke conflict. The key value is stored in the address 50H, 51H, 52H. If the key value read is 01H, 01H, 01H, it indicates that there is an error on the keyboard. The reason for the error may be that more than three keys are pressed at the same time or there is a key position conflict between the three keys pressed at the same time. The location of the key value is arbitrary (address 50H, any one of 51H, 51H, 52H). 00H indicates that the key is released, and the size of the key value corresponds to the position of the key in the picture above (If K36 is pressed, the read key value is 36H).

6.3 PWM and BZ and GPIO Extension

KS0-KS4, KI0-KI6 can be specified separately as a normal GPIO pin, and when used as a GPIO, the corresponding keys are invalid.

Address 48H Bit0 to Bit6 corresponds to KI0 to KI6 GPIO enabled, if it is 1, then the corresponding KI pin is used as GPIO. The Bit0 to Bit6 of the address 4AH is the output enable when KI0 to KI6 is used as the GPIO. When it is 1, the output enable is turned on, and the output value is the Bit0 to Bit6 of the address 4EH. When reading the address 4EH, it reads the state of the KI0 to KI6 pin. The address Bit0 to Bit6 of 4CH is the pull-up enable when KI0 to KI6 is used as GPIO, and when it is 1.

Address 49H Bit0 to Bit4 corresponds to KS0 to KS4 GPIO enabled, if 1, then the corresponding KS pin is used as GPIO. The Bit0 to Bit4 of the address 4BH is the output enable when KS0 to KS4 is used as the GPIO. When it is 1, the output enable is turned on, and the output value is the Bit0 to Bit4 of the address 4FH. When reading the address 4FH, it reads the state of the KS0-to-KS4 pin, where Bit5, Bit6 is the state of the PWM, BZ pin. The address Bit0 to Bit4 of 4DH is the pull-up enable when KS0 to KS4 is used as GPIO, and when it is 1.

The Bit2 of address 41H is the PWM enable bit, which enables PWM output at position 1 and turns off when it is set to 0.

The Bit3 of address 41H is the BZ enable bit, which enables BZ output at position 1 and turns off when it is set to 0.

PWM and BZ can also be designated as normal GPIO when the corresponding enable level is turned off. The Bit5, Bit6 of the address 4BH is the output enable when PWM, BZ is used as the GPIO. When it is 1, the output enable is turned on, and the output value is the Bit5, Bit6 value of the address 4FH. When the address 4FH is read, the read Bit5, Bit6 is the state of the PWM, BZ pin. The Bit5, Bit6 of the address 4DH is the pull-up enable when PWM, BZ is used as GPIO, and when it is 1.

Address 45H is the PWM configuration register (valid only from 0 to 63) and is used to set the pulse width of PWM.

Configuration Value	Pulse width setting of PWM
00H	Always 0
01H~3EH	1/64~62/64
3FH	Always 1

Address 46H is the BZ configuration register (valid only for Bit1, Bit0) and is used to set the frequency of BZ.

Configuration Value	Frequency setting of BZ
00H	OFF
01H	Low frequency (4KHz, Fosc/32)
02H,03H	High frequency (8KHz, Fosc/16)

6.4 Serial Port Interface

CH463's 2-wire serial interface consists of three signal lines: the serial data clock input line SCL, the serial data input and output line SDA, and the optional interrupt output line INT. Among them, SCL is an input signal line with pull-up, which defaults to high level; SDA is a quasi-bi-directional signal line with pull-up, which defaults to high level; and INT is an open-drain output signal line with pull-up, which defaults to high level.

SDA is used for serial data input and output, high level represents bit data 1, low level indicates bit data 0, the order of serial data input is high bit first, low bit last.

The SCL is used to provide a serial clock, and the CH463 inputs data from the SDA during the high level behind its rising edge and outputs data from the SDA during the low level behind its falling edge.

INT is used for keyboard interrupt output.

The SDA falling edge that occurs when the SCL is high is defined as the start signal of the serial interface, and the SDA rising edge that occurs when the SCL is high is defined as the stop signal of the serial interface. CH463 receives and analyzes commands only after the startup signal is detected. Therefore, when the resource of SDA pin is tight, SCL pin can be shared with other interface circuits as long as the state of SCL pin is kept unchanged.

There are two ways of communication between single-chip microcomputer and CH463, one is write operation, which is used to output data, and the other is read operation, which is used to input data. The specific process can refer to the instructions in the example program.

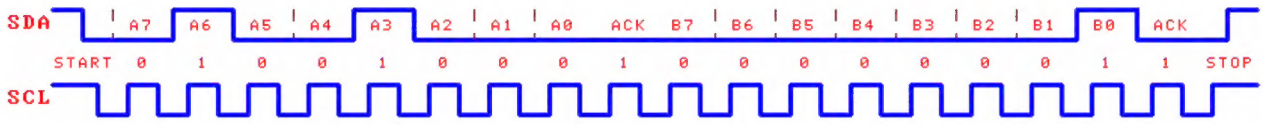
The write operation includes: output start signal, output byte 1, reply 1, output byte 2, reply 2, (output byte n, reply

n) output stop signal. Among them, the start signal and stop signal are described above, the reply signal is 0, and the output byte contains 8 data bits, that is, one byte of data.

The read operation includes: output start signal, output byte 1, reply 1, input byte 2, reply 2, (input byte n, reply n, the last reply is not given, otherwise the stop signal may not be generated) the output stop signal. Among them, the start signal and stop signal are described above, the reply signal is 0, and the output bytes and input bytes contain 8 data bits, that is, one byte of data.

In the above, the first byte of output is address plus command (read or write), the first 7 bits are address signal (high bit comes first), the last bit indicates read or write (1 indicates read, 0 indicates write), byte 2 is the data written or read, each operation byte address is automatically added 1, the direction of the reply signal is opposite to the direction of the data signal in front of him.

The following figure is an example of a write operation. Byte 1 is 01001000B, or 48H, and byte 2 is 00000001B, or 01H.



7. Parameters

7.1 Absolute Maximum Value

Name	Parameter description	Min.	Max.	Unit
TA	Ambient temperature during operation	-40	85	℃
TS	Ambient temperature during storage	-55	125	℃
VCC	Supply voltage (VCC connects to power, GND to ground)	-0.5	5.5	V
VIO	Voltage on the input or output pins	-0.5	VCC+0.5	V
VLCD	LCD voltage	1.5	5	V

7.2 Electrical Parameters (Test conditions: TA=25℃, VCC=5V)

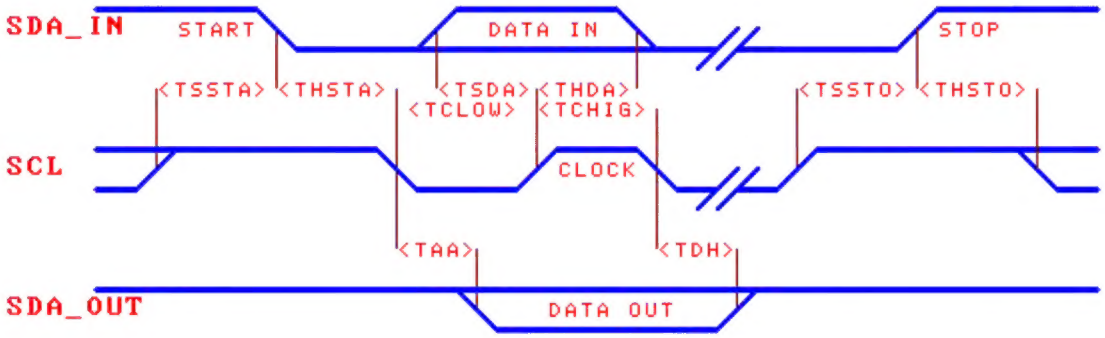
Name	Parameter description	Min.	Typ.	Max.	Unit
VCC	Power supply voltage	3	5	5.5	V
VLCD	LCD voltage	0	VCC	5	V
ICC	Supply current (LCD on, I/O internal pull-up)	100	200		uA
Islp5	5V static current (LCD off, I/O internal pull-up)		25	50	uA
Islp3	3.3V static current (LCD off, I/O internal pull-up)		12	30	uA
VIL	Low level input voltage			0.7	V
VIH	High level input voltage	2.0			V
Iox	LCD SEG and COM drive current		100		uA
VOL	PWM, BZ, KI and KS low level output voltage (-2mA)			0.5	V
VOH	PWM, BZ, KI and KS high level output voltage (2mA)	VCC-0.5			V

7.3 Internal Timing Parameters (Test conditions: TA=25℃, VCC=5V)

(Note: The timing parameters in this table are all multiples of the Fosc cycle, and the frequency of the built-in clock Fosc may be affected by the power supply voltage)

Name	Parameter description	Min.	Typ.	Max.	Unit
TPR	Power on reset time	3	10	50	mS
Fosc	Oscillation frequency	50	128	250	KHz
Fpwm	PWM frequency		Fosc/2		KHz
TKS	Keyboard scanning key response time	5	15	50	mS

7.4 Interface Timing Parameters (Test conditions: TA=25 ℃, VCC=5V, see attached drawing)

Name	Parameter description	Min.	Typ.	Max.	Unit
TSSTA	Setup time of SDA falling edge start signal	200			nS
THSTA	Hold time of SDA falling edge start signal	200			nS
TSSTO	Setup time of SDA rising edge stop signal	200			nS
THSTO	Hold time of SDA rising edge stop signal	200			nS

TCLOW	Low level width of SCL clock signal	200			nS
TCHIG	High level width of SCL clock signal	200			nS
TSDA	Setup time of SDA input data to SCL rising edge	30			nS
THDA	Hold time of SDA input data to SCL rising edge	10			nS
TAA	Delay SDA output data to SCL falling edge	5	100		nS
TDH	Delay of invalid SDA output data to SCL falling edge	5	100		nS
Rate	Average data transmission rate	0		2M	bps